International Journal of Management, IT & Engineering
Vol. 9 Issue 1, January 2019,
ISSN: 2249-0558 Impact Factor: 7.119
Journal Homepage: http://www.ijmra.us, Email: editorijmie@gmail.com
Double-Blind Peer Reviewed Refereed Open Access International Journal - Included in the International Serial Directories Indexed & Listed at: Ulrich's Periodicals Directory ©, U.S.A., Open J-Gage as well as in Cabell's Directories of Publishing Opportunities, U.S.A

A Novel Programmable 16 Bit ALU Using Vedic Multiplier and Kogge-Stone Adder

Mr.B.Venkateshwarlu *
Dr. S. Kishore Reddy **
Dr G Sai Kumar***

*** M.Tech Student,**
VLSI design ,ECE,Avanthi institute of engineering and technology

Abstract

Significant contributions have been made in the literature towards the design of arithmetic units, however, there are not many efforts directed towards the design of 16 bit ALU. In this paper, a novel programmable 16 bit ALU using Vedic multiplier and Kogge-Stone adder is presented and verified, and its implementation in the design Arithmetic Logic Unit is demonstrated. Then, implementations of 16 bit Kogge-Stone adders, Vedic multiplier are analysed and compared in terms of delay. The performance characteristics analysis is carried out in Xilinx environment

Keywords:

Vedic Adder;
Koggestone Adder;
Wallace tree multiplier;
Fourth keyword;
Fifth keyword.

Author correspondence:

1. Introduction

Vedic Sutras apply to and cover almost every branch of Mathematics. They apply even to complex problems involving large number of mathematical operations. Application of the Sutras saves a lot of time and effort in solving the problems, compared to the form al methods presently in vogue. Though the solutions appear like magic, the application of the Sutras i perfectly logical an drational.The computation made on the computers follows, in a way, the principle suddenly in the Sutras. The Sutras provide not only methods of calculation, but also ways of thinking for their application

Application of the Sutras improves the computational skills of the learners in a wide area of problems, ensuring both speed and accuracy, strictly based on logical reasoning. Application of the Sutras to specific problems involves rational thinking, which,in the process, helps improve intuition that is the bottom- line of the mastery of the mathematical geniuses of the past and the present such as Aryabhatta, Bhaskaracharya, Srinivasa Ramanujan,etc.Multiplier implementation using FPGA has already been reported using different multiplier architectures but the performance of multiplier was improved in proposed design.

What we call "Vedic mathematics" is comprised of sixteen simple mathematical formulae from the Vedas.

1. EkadhikenaPurvena
2. NikhilamnavathascaramamDasatah
3. UrdhvaTiryagbhyam
4. ParavartyaYojayet

***** Assistant Professor, ECE dept, Avanthi institute of engineering and technology,Hyderabad***
Kishorereddy416@gmail.com
*** ***Assistant Professor, ECE dept, Avanthi institute of engineering and technology,hyderabad***

5. SunyamSamyaSamuccaye
6. AnurupyeSunyamanyat
7. SankalanaVyavakalanabhyam
8. Puranapuranabhyam
9. CalanaKalanabhyam
10. EkanyunenaPurvena
11. Anurupyena
12. Adyamadyenantyamantyena
13. YavadunamTavadunikrtyaVargancaYojayet
14. AntyayorDasakepi
15. Antyayoreva
16. GunithaSamuccayah

Different Types of Multipliers:

An efficient multiplier should have following characteristics:-
Accuracy:A good multiplier should give correct result.
Speed: Multiplier should perform operation at high speed.
Area:A multiplier should occupy less number of slices and LUTs.
Power:Multiplier should consume less power.
Multiplication process has three main steps
Partial product generation.
Partial product reduction.
Final addition

For the multiplication of an n-bit multiplicand with an mbit multiplier, m partial products are generated and product formed is n + m bits long. Here we discuss about four different types of multipliers which are
Combinational multiplier.
Wallace tree multiplier.
Array multiplier.
Sequential multiplier

2. Design& Implementation Block Digram Of The Proposed Deign

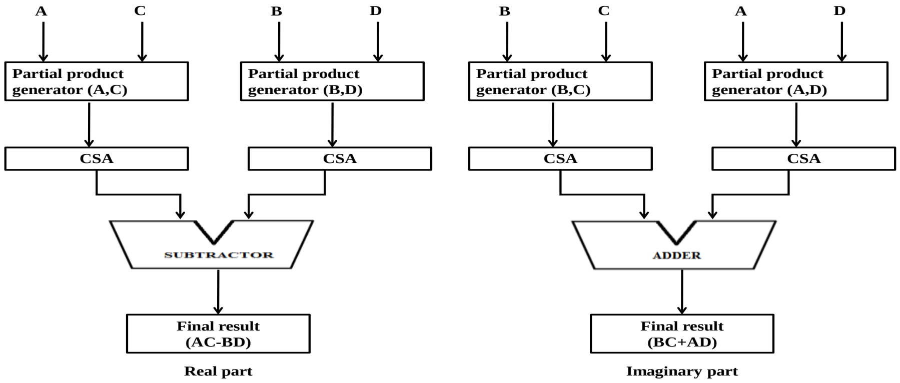

A
C
B
D
B
C
A
D
Partial product generator (A,C)
Partial product generator (B,D)
Partial product generator (B,C)
Partial product generator (A,D)
CSA
CSA
CSA
CSA
SUBTRACTOR
ADDER
Final result (AC-BD)
Final result (BC+AD)
Real part
Imaginary part

Figure 1. an *8 bit* Vedic *multiplier*

DESCRIPTION:

Multiplication is the process of adding a number of partial products. Multiplication algorithms differ in terms of partial product generation and partial product addition to produce the final result.Higher throughput arithmetic operations are important to achieve the desired performance in many real time signal and image processing applications. With time applications, many researchers have tried to design multipliers which offer either of the following- low power consumption, high speed, regularity of layout and hence less area or even grouping of them in multiplier.

Complex number arithmetic computation is a key arithmetic feature in modem digital communication and optical systems. Many algorithms based on convolutions, correlations, and complex filters require complex number multiplication, complex number division, and high-speed inner-products. Among these computations, complex number multipliers and complex number inner-products are becoming more and more demanded in modem digital communication, modem optical systems, and radar systems.

Multiplication is an essential operation for high speed hardware implementation of complex number computation. To compute the product of two complex numbers, the conventional method is to use four binary multiplications, one addition, and one subtraction.

A = A,+ JA, AND B=B,+ JB,

Multiplication of A and B is given by

AXE = ARB, - A,B, + j(A,B, +A$,)

The paper is organized as follows. In section 2, Vedic multiplication method based on Urdhava Tiryakbhyam sutra is discussed. Section 3 deals with the design of the above said multiplier. Section 4summarizes the experimental results obtained, while section 5 presents the conclusions of the work.

While implementing complex number multiplication, the multiplication system can be divided into two main components giving the two separate results known as real part (R) and imaginary part (I).

R + j I = (A + j B) (C + j D)

Gausses algorithm for complex number multiplication gives two separate equations to calculate real and imaginary part of the final result. From equation (1) the real part of the output can be given by (AC - BD), and the imaginary part of the result can be computed using (BC + AD). Thus four separate multiplications and are required to produce the real as well as imaginary part numbers.

Multiplication process is the critical part for any complex number multiplier design. There are three major steps involved for multiplication. Partial products are generated in first step. In second step partial product reduction to one row of final sums and carries is done .Third and final stage adds the final sums and carries based onRadix-4modified Booth algorithm consists of two main blocks known as MBE (Modified Booth Encoding) and partial product generator as shown in Fig. Wallace Tree CSA structures have been used to sum the partial products in reduced time. In this regard, combining both algorithms in one multiplier, we can expect a significant reduction in computing multiplications

KOGGESTONE ADDER

KSA is a parallel prefix form carry look ahead adder. It generates carry in O (logn) time and is Widely considered as the fastest adder and is widely used in the industry for high performance arithmetic circuits. In KSA, carries are computed fast by computing them in parallel at the cost of increased area.

Theory:

The complete functioning of KSA can be easily comprehended by analyzing it in terms of three Distinct parts:

1. Pre processing:

This step involves computation of generate and propagate signals corresponding too each pair of bits in A and B. These signals are given by the logic equations below:

pi = Ai *xor* Bi

gi = Ai *and* Bi

2. Carry look aheadnetwork:

This block differentiates KSA from other adders and is the main force behind its high Performance. This step involves computation of carries corresponding to each bit. It uses group propagate and generate as intermediate signals which are given by the logic Equations below:

Pi:j = Pi:k+1 *and Pk:j*

Gi:j = Gi:k+1 *or* (Pi:k+1 *andGk:j*)

3. Post processing

This is the final step and is common to all adders of this family (carry look ahead). It involves computation of sum bits. Sum bits are computed by the logic given below:
Si = pi xor Ci-1
Illustration
The working of KSA can be understood by the following Fig. 1 which corresponds to 4-bit KSA. 4-bit KSA is shown for simplicity.
Layout
The complete layout is shown in Fig. 6. Technology used was AMS 0.35um c35b4. Layout was done using Cadence Virtuoso Layout Editor. The DRC and LVS runs were successfully done.

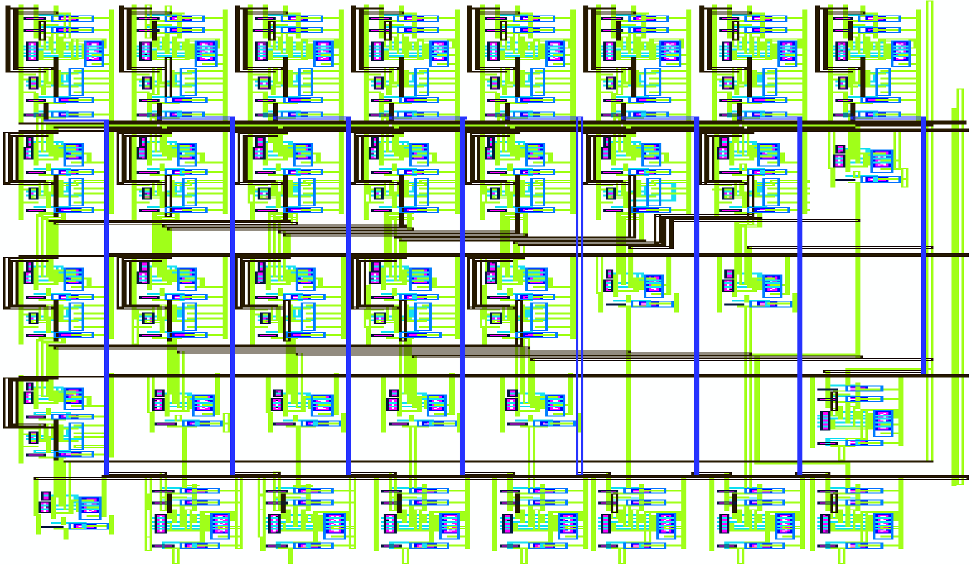


Figure 2. AMS 0.35 um *Layout*

3. SIMULATION RESULTS
Following specifications were achieved:

- Max frequency = 374.94 MHz
- Area = 440 µm X 300 µm = 0.132 mm^2
- Power = 460

We designed and implemented 8 bit Kogge-Stone Tree Adder that operates at 375 MHz(fmax) and complete layout takes an area of 440 X 300 um^2.

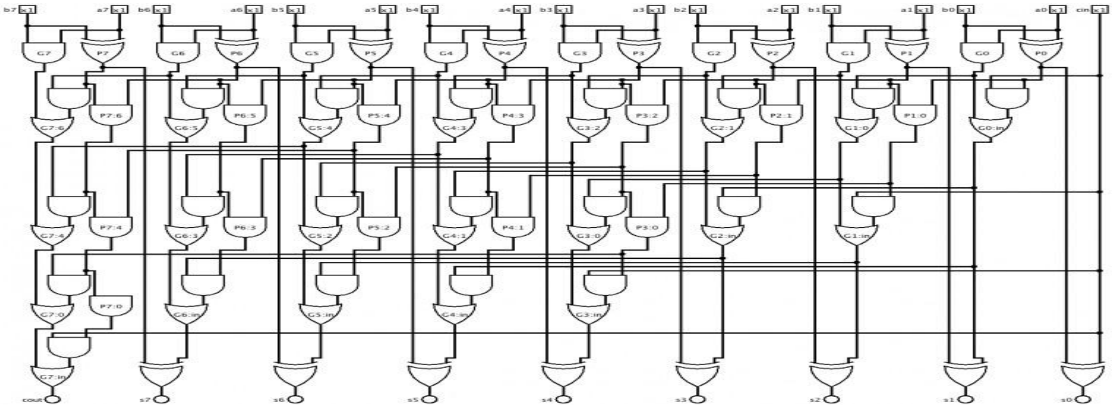
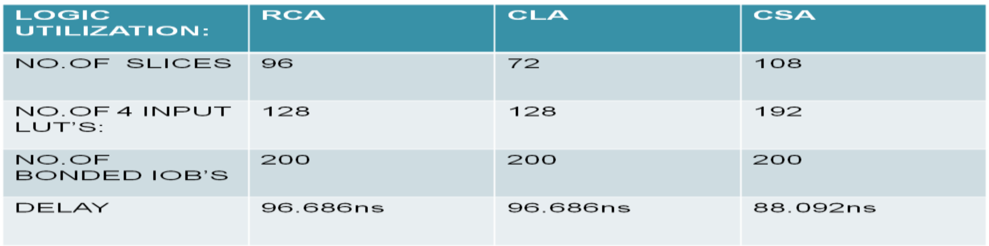


Figure 3. *Kogge Stone Adder*



LOGIC UTILIZATION:	RCA	CLA	CSA
NO.OF SLICES	96	72	108
NO.OF 4 INPUT LUT'S:	128	128	192
NO.OF BONDED IOB'S	200	200	200
DELAY	96.686ns	96.686ns	88.092ns

Table 1. *Synthesis report*

CONCLUSION

The design has been made to reduce the propagation delay With 25% compared to existing multiplier. The propagation delay for proposed 8-bit Vedic multiplier is found to be 80ns. There complex numbers is much more efficient than compared with Vedic multiplier and execution time will be speed.

These paper presents a highly efficient method of multiplication-UrdhvaTiryakhyama based sutra on Vedic mathematics. It is a method for hierarchical multiplier design offered by Vedic methods. The computational path delay for proposed 8 x 8 bit Vedic multiplier is much more efficient than array and booths multiplier in terms of execution time. An awareness of Vedic mathematics can be efficiently increased if it is included in engineering education.

REFERENCES

1) PrabirSaha, Arindam Banerjee, Partha Bhattacharyya, AnupDandapat, “High speed ASIC design of complex multiplier using vedic mathematics” , Proceeding of the 2011 IEEE Students' Technology Symposium 14-16 January, 2011, lITKharagpur, pp. 237-241.

2) ShamsiahSuhaili and Othman Sidek, “Design and implementation of reconfigurable alu on FPGA”, 3rd International Conference on Electrical & Computer Engineering ICECE 2004, 28-30 December 2004, Dhaka, Bangladesh, pp.56- 59.

3) SumitVaidya and Deepak Dandekar, “Delay-power performance comparison of multipliers in vlsi circuit design”, International Journal of Computer Networks& Communications (IJCNC), Vol.2, No.4, July 2010, pp.47-56.

4) P. Mehta, and D. Gawali, "Conventional versus Vedic mathematical method for Hardware implementation of a multiplier," in Proceedings IEEE International Conference on Advances in Computing, Control, and Telecommunication Technologies, Trivandrum, Kerala, Dec. 28- 29, 2009, pp. 640-642.

5)J. S. S. B. K. T. Maharaja, Vedic mathematics, Delhi: MotilalBanarsidass Publishers Pvt Ltd,(2010).

6) PrabirSaha, Arindam Banerjee, Partha Bhattacharyya, AnupDandapat, “High speed ASIC design of complex multiplier using vedic mathematics” , Proceeding of the 2011 IEEE Students' Technology Symposium 14-16 January, 2011, lITKharagpur, pp. 237-241.

7) ShamsiahSuhaili and Othman Sidek, “Speed Comparison of 16x16 Vedic Multipliers ICECE 2004, 28-30 December 2004, Dhaka, Bangladesh, pp.56-59.

8) SumitVaidya and Deepak Dandekar, “Delay-power performance comparison of multipliers in vlsi circuit design”, International Journal of Computer etworks& Communications (IJCNC), Vol.2, No.4, July 2010, pp.47-56.